22.3.2021

A Report

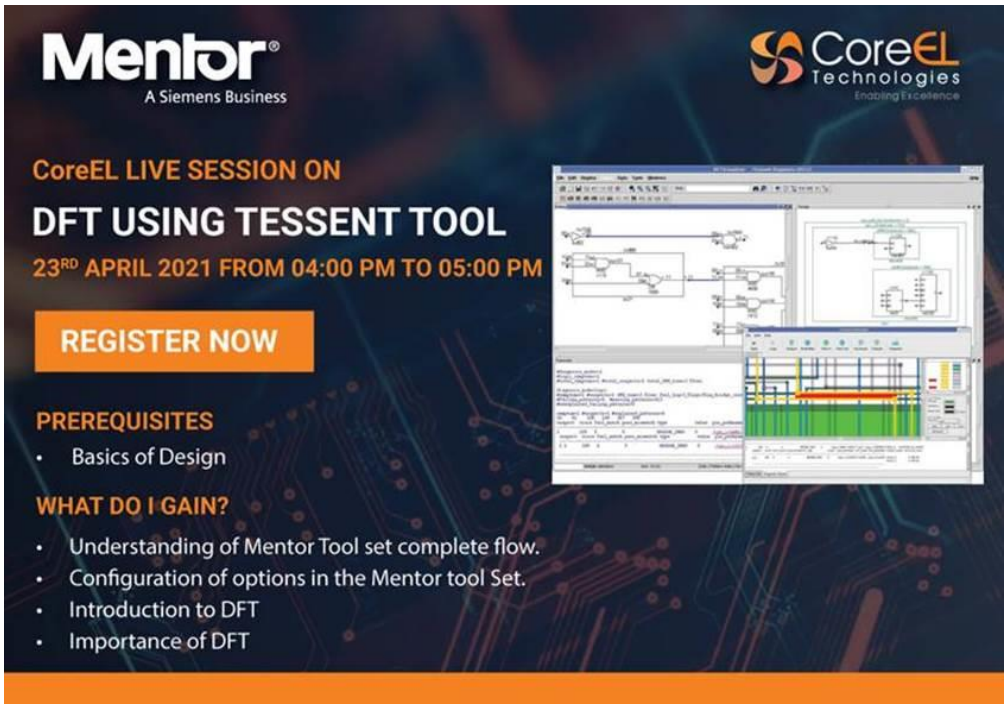
On

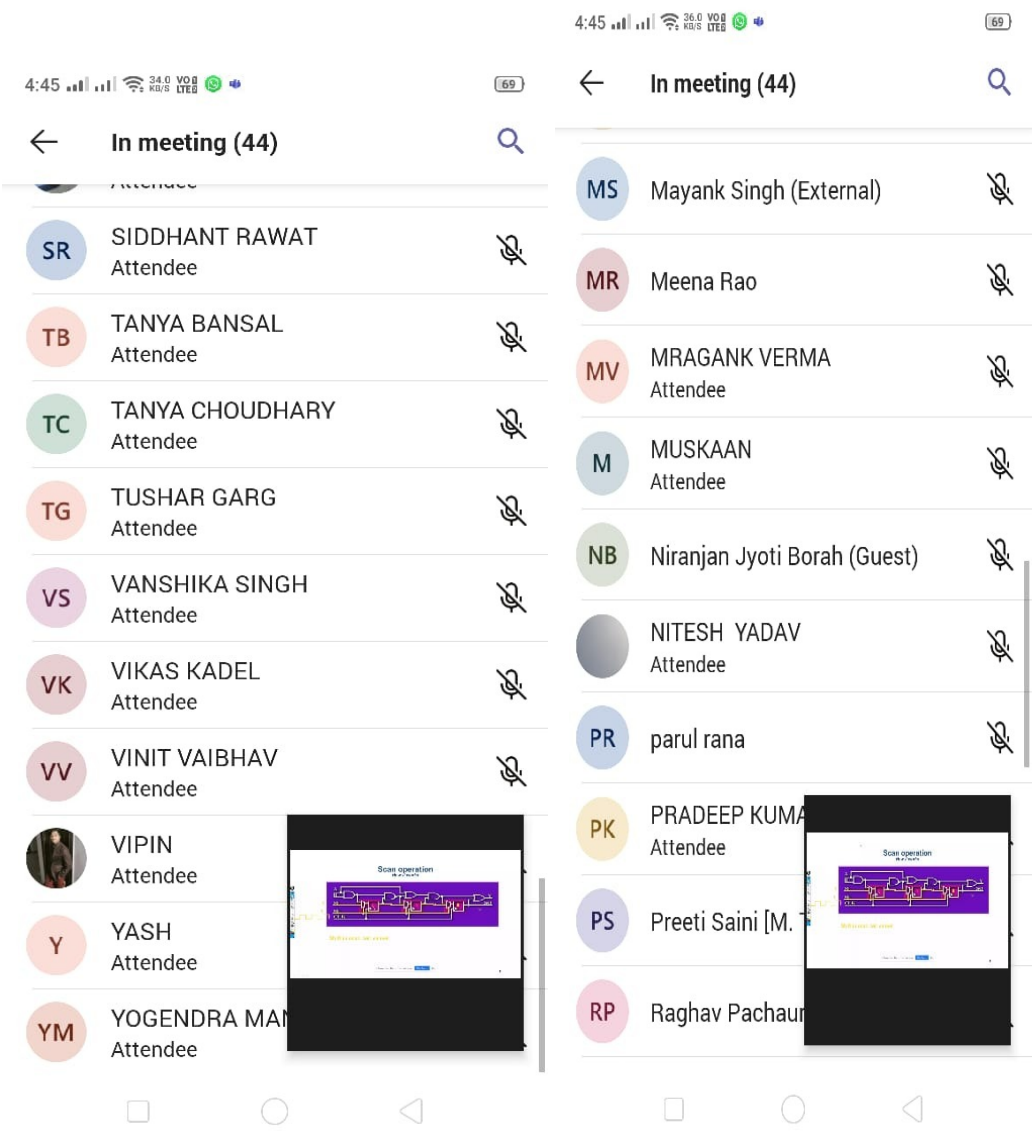
An expert talk on "DFT using Tessent tool" by CoreEL Technologies
Date : 23rd April, 2021 ; Time : 4:00 – 5:00 pm
No. of attendees from MSIT : 44

An expert talk has been organized by ECE Deptt. on "DFT using Tessent tool" for the faculty and students of 2nd and 3rd year of ECE branch on 23rd April, 2021 from 4:00pm to 5:00pm on Microsoft teams. Dr. Sudesh Pahal in coordination with Mr. Raghav Pachaury, CoreEL Technologies conducted the program. Five faculty members along with 39 students registered for the session. The session was focussed on EDA Solutions for IC/ASIC Design & Verification – Semi - Custom Design Flow demonstration (RTL to GDSII Flow), Basics of Design for Testability, Need For DFT and DFT with Tessent tool. It was very useful for Faculty members and Research students interested in up-skilling and Engineering (UG/PG) graduates aspiring to build a career in VLSI industry as analog engineers.

The audience gained benefits in terms of Understanding of Mentor Tool set complete flow, Configuration of options in the Mentor tool Set, Introduction to DFT and Importance of DFT

At the end, the Students also participated during the QA session and they were also asked to share their interest and vision with the subject to bring in more clarity to choose the right language and career path. Further the webinar was concluded with vote of thanks by the coordinator.





Dr. Sudesh Pahal

Coordinator